flowing in the second configuration from the electrode structure to the charge storing node and vice versa in response to given voltages applied to the device so as to charge and discharge the node selectively through the lamination structure, and wherein charge is stored on the node in the first configuration.

3. (Amended) A memory device comprising:

a path for charge carriers;

a charge storing node to produce a field which alters a conductivity of the path; and

a lamination structure including an insulating film and a semiconductor film, the lamination structure being disposed between an electrode structure and the charge storing node,

the lamination structure having an energy band profile that is changeable between a first configuration in which a barrier height of the energy band profile is high and a second configuration in which the barrier height of the energy band profile is low, an electric current flowing in the second configuration between the electrode structure and the charge storing node and vice versa in response to given voltages applied to the device so as to charge and discharge the node selectively through the lamination structure, and wherein charge on the node is stored in the first configuration.

5. (Amended) A memory device comprising:

a source-drain path for charge carriers;

a charge storing node to produce a field which alters a conductivity of the source-drain path; and

a lamination structure including an insulating film and a semiconductor film, the lamination structure being disposed between electrode structure and the charge storing node,

the lamination structure having an energy band profile that is changeable between a first configuration in which a barrier height of the energy band profile is high and a second configuration in which the barrier height of the energy band profile is low, an electric current flowing in the second configuration from the electrode structure to the charge storing node and vice versa in response to given voltages applied to the device so as to charge and discharge the node selectively through the lamination structure, and wherein charge on the node is stored in the first configuration.

15. (Amended) A memory device comprising:

a charge storage node,

an electrode structure, and

a barrier structure between the electrode structure and the charge storage node, the barrier structure providing a variable internal electrostatic barrier potential configurable by an external bias to provide selectively a relatively low barrier height for which charge carriers can pass from the electrode structure to the charge storage node and vice versa to charge and discharge the node, and a relatively high barrier height to store charge carriers on the charge storage node.

21. (Amended) A memory device comprising:

a substrate;

an array of memory cells configured on the substrate; and

a plurality of word lines and data lines extending between the cells, the word lines being operable to receive cell selection signals;

each of the memory cells comprising a charge storage node, an electrode forming part of one of the data lines, and a barrier structure between the electrode and the charge storage node, the barrier structure providing a variable internal electrostatic barrier potential configurable selectively in response to an external bias provided by a selection signal applied to one of the word lines to provide a relatively low barrier height for which charge carriers can pass between the electrode structure and the charge storage node for charging and discharging the node, and a relatively high barrier height to store charge carriers on the charge storage node.

35. (Amended) A method of fabricating a memory device, comprising: forming a charge storage node, an electrode structure and a barrier structure so that the barrier structure is disposed between the electrode structure and the charge storage node, and such that the barrier structure presents an internal relatively high electrostatic barrier potential that retains charge on the storage node, the barrier being lowerable by an external voltage applied to the electrode structure to allow charge carriers to flow from the electrode structure to the charge storage node and vice versa, to charge and discharge the node.

45. (Amended) A memory device comprising:

a substrate,

an array of memory cells configured on the substrate,

a plurality of word lines and data lines extending between the cells,

each of the memory cells comprising a charge storage node, an electrode structure coupled to one of the data lines and a barrier structure between the electrode structure and the charge storage node, the barrier structure providing an internal electrostatic barrier potential of a relatively high barrier height to store charge carriers on the charge storage node, the barrier being configurable selectively in response to an external bias applied to one of the word lines to provide a relatively low barrier height for which charge carriers can pass between the electrode structure and the charge storage node,

reading circuitry to read the level of charge stored on the charge storage nodes of the cells individually, and

writing circuitry to write charge onto the charge storage nodes of the cells individually.

Please add new claims 50-58.

50. (NEW) A memory device comprising:

a substrate,

an array of memory cells configured on the substrate,

an electrically insulating layer on the substrate,

a plurality of word lines and data lines extending between the cells,

each of the memory cells comprising a barrier structure and a memory node, the barrier structure overlying the insulating layer and providing an internal electrostatic barrier potential of a relatively high barrier height to keep voltage on the memory node, the barrier being configurable selectively in response to an external bias applied to one of the word lines to provide a relatively low barrier height whereby a current flows through the barrier structure to change the voltage on the memory node,

reading circuitry to read the level of charge stored on the memory nodes of the cells individually, and

writing circuitry to write charge onto the charge storage nodes of the cells individually.

51. (NEW) A memory device according to claim 50, wherein the substrate is comprised of silicon, the insulating layer is selected from a group comprising an oxide and a nitride of silicon.

52. (NEW) A memory device according to claim 50, wherein the memory node is formed of a conductive silicon material.

cont'd
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53. (NEW) A memory device according to claim 50, wherein the barrier structure is formed of polysilicon material.

54. (NEW) A memory device according to claim 50, including a control gate configured to control the barrier height presented by the barrier structure to a current that flows to and from the memory node.

55. (NEW) A memory device according to claim 50, wherein the current that flows to and from the memory node, flows vertically through the barrier structure.

56. (NEW) A memory device comprising:

a substrate,

an array of memory cells configured on the substrate,

an electrically insulating layer on the substrate,

a plurality of word lines and data lines extending between the cells,

each of the memory cells comprising an electrode, a memory node, a barrier structure between the electrode and the memory node, and a control gate, the barrier structure overlying the insulating layer and providing an internal electrostatic barrier potential of a relatively high barrier height to keep voltage on the memory node, the control gate being operable to receive an external voltage bias applied to one of the word lines so as to apply a field to the barrier structure resulting in a relatively low barrier height whereby a current flows through between the electrode and the memory node through the barrier structure to change the voltage on the memory node, and

reading circuitry to read the level of charge stored on the memory nodes of the cells individually.

57. (NEW) A memory device comprising:

a substrate,

a horizontal transistor formed in the substrate, and

a vertically configured controllable conduction device overlying the horizontal transistor, comprising an electrode, a memory node, a barrier structure between the electrode and the memory node, and a control gate, the barrier structure providing an internal electrostatic barrier potential of a relatively high barrier height to keep voltage on the memory node, the control gate being operable to receive an external voltage bias whereby the barrier structure presents a relatively low barrier height and a current flows between the electrode and the memory node through the barrier structure so as to change the voltage on the memory node.

58. (NEW) A method of fabricating a semiconducto9r device, comprising:

providing a substrate, providing an electrically insulating layer on the substrate, fabricating an array of memory cells, providing a plurality of word lines and data lines extending between the cells, each of the memory cells comprising a barrier structure and a memory node, the barrier structure overlying the insulating layer and providing an internal electrostatic barrier potential of a relatively high barrier height to keep voltage on the memory node the barrier being configurable selectively in response to an external bias applied to one of the word lines to provide a relatively low barrier height whereby a current flows through the barrier structure to change the voltage on the memory node, providing reading circuitry to read the level of charge stored on the memory nodes of the cells individually, and fabricating writing circuitry to write charge onto the charge storage nodes of the cells individually.

REMARKS

Claims 1-12 and 15-58 are pending. By this Amendment, claims 13 and 14 are cancelled, claims 1, 3, 5, 15, 21, 35 and 45 are amended and new claims 50-58 are added. It is noted that while claims 35-38 are non-elected, they are still pending.